Appendix A – Listing of Claims in Clean Form

Claims 1 - 15 (Canceled)

Claim 16 (Currently Amended)

An internal switching fabric within an System-on-Chip (SOC) that routes signals between requestors and addressable targets, comprising:

one or more requestor connection ports that couple to one or more requestors;

one or more target connection ports that couple to one or more addressable targets wherein each said addressable target is mapped to a unique predefined address space; and

one or more decoder/router elements that couple to said requestor connection ports and said target connection ports, each said decoder/router element receives a request from a single said requestor in the requester bus protocol, determines which said addressable target is the designated target using an internal system memory map, and route said request to said designated target in the target bus protocol, wherein each said decoder/router element is coupled to said single said requestor through a single said requestor port.

Claim 17 (Currently Amended)

The claim of claim 16 further comprising one or more arbiters one that couple to said decoder/router elements and said target connection ports and arbitrates said requests between said requestors and said designated targets.

Claim 18 (Previously Added)

The claim of claim 16 wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requestor port and an independently accessible target port.

Claim 19 (Previously Added)

The claim of claim 16 wherein said request routed to said designated target by said decoder/router element further comprises a registered, point-to-point signal that further comprises a plurality of pipeline stages.

Claim 20 (Currently Amended)

An method to manufacture an internal switching fabric within an System-on-Chip (SOC) that routes signals between requestors and addressable targets, comprising:

coupling one or more requestor connection ports to one or more requestors;

coupling one or more target connection ports to one or more addressable targets wherein each said addressable target is mapped to a unique predefined address space; and

coupling one or more decoder/router elements to said requestor connection ports and said target connection ports, said decoder/router element receives a request from a single said requestor in the requester bus protocol, determines which said addressable target is the designated target using an internal system memory map, and routes said request to said designated target in the target bus protocol, wherein each said decoder/router element is coupled to said single said requestor through a single said requestor port.

Claim 21 (Currently Amended)

The claim of claim 20 further comprising one or more arbiters one that couple to said decoder/router elements and said target connection ports and arbitrates said requests between said requestors and said designated targets.

Claim 22 (Previously Added)

The claim of claim 20 wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requestor port and an independently accessible target port.

Claim 23 (Previously Added)

The claim of claim 20 wherein said request routed to said designated target by said decoder/router element further comprises a registered, point-to-point signal that further comprises a plurality of pipeline stages.

Claim 24 (Currently Amended)

A method to use an internal switching fabric within an System-on-Chip (SOC) that routes signals between requestors and addressable targets, comprising:

providing one or more requestor connection ports that couple to one or more requestors;

providing one or more target connection ports that couple to one or more addressable targets wherein each said addressable target has a unique address space; and

providing one or more decoder/router elements that couple to said requestor connection ports and said target connection ports, said decoder/router element receives a request from a single said requestor in the requester bus protocol, determines which

said addressable target is the designated target using an internal system memory map, and routes said request to said designated target in the target bus protocol, wherein each said decoder/router element is coupled to said single said requestor through a single said requestor port.

Claim 25 (Currently Amended)

The claim of claim 24 further comprising one or more arbiters one that couple to said decoder/router elements and said target connection ports and arbitrates said requests between said requestors and said designated targets.

Claim 26 (Previously Added)

The claim of claim 24 wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requestor port and an independently accessible target port.

Claim 27 (Previously Added)

The claim of claim 24 wherein said request routed to said designated target by said decoder/router element further comprises a registered, point-to-point signal that further comprises a plurality of pipeline stages.

Claim 28 (New)

The claim of claim 16 wherein said unique predefined address space further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system.

Claim 29 (New)

The claim of claim 16 wherein one of said decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets.

Claim 30 (New)

The claim of claim 20 wherein said unique predefined address space further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system.

Claim 31 (New)

The claim of claim 20 wherein one of said decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets.

Claim 32 (New)

The claim of claim 24 wherein said unique predefined address space further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system.

Claim 33 (New)

The claim of claim 24 wherein one of said decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets.

Claim 34 (New)

A program storage device readable by a computer that tangibly embodies a program of instructions executable by the computer to perform a method to use an internal switching fabric within an System-on-Chip (SOC) that routes signals between requestors and addressable targets, comprising:

providing one or more requestor connection ports that couple to one or more requestors;

providing one or more target connection ports that couple to one or more addressable targets wherein each said addressable target has a unique address space; and

providing one or more decoder/router elements that couple to said requestor connection ports and said target connection ports, said decoder/router element receives a request from a single said requestor in the requester bus protocol, determines which said addressable target is the designated target using an internal system memory map,

and routes said request to said designated target in the target bus protocol, wherein each said decoder/router element is coupled to said single said requestor through a single said requestor port.

Claim 35 (New)

The claim of claim 34 further comprising one or more arbiters one that couple to said decoder/router elements and said target connection ports and arbitrates said requests between said requestors and said designated targets.

Claim 36 (New)

The claim of claim 34 wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requestor port and an independently accessible target port.

Claim 37 (New)

The claim of claim 34 wherein said request routed to said designated target by said decoder/router element further comprises a registered, point-to-point signal that further comprises a plurality of pipeline stages.

Claim 38 (New)

The claim of claim 34 wherein said unique predefined address space further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system.

Claim 39 (New)

The claim of claim 34 wherein one of said decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets.